Claims 1-5 and 8-12 are rejected under 35 U.S.C. § 102 for lack of novelty as evidenced by Lee, U.S. Patent No. 6,277,705

In the third enumerated paragraph of the Office Action, the Examiner asserted that Lee discloses a semiconductor device corresponding to that claimed. This rejection is respectfully traversed.

The factual determination of lack of novelty under 35 U.S.C. § 102 requires the identical disclosure in a single reference of each element of a claimed invention, such that one having ordinary skill in the art would have recognized that the identically claimed invention is within the public domain.[1] Furthermore, the Examiner must also establish that the applied reference identically discloses *each* feature of the claimed invention.[2] As part of this analysis, the Examiner must (a) identify the elements of the claims, (b) determine the meaning of the elements in light of the specification and prosecution history, and (c) identify corresponding elements disclosed in the allegedly anticipating reference.[3] Claim 1, as amended, recites that a predetermined void separates a plug from a second interconnection, and this limitation can be illustrated, for example, in Fig. 1 of Applicant's disclosure. This limitation, however, is neither disclosed nor suggested by Lee.

The conductive layer 20 of Lee is formed directly on the conductive plug 20, and the voids 26a, 26b of Lee are merely adjacent to the conductive layer 22 and the conductive plug 20. As such, the voids 26a, 26b of Lee cannot separate the conductive plug 20 from the conductive layer

[1] ATD Corporation v. Lydall, Inc., 159 F.3d 534, 48 USPQ2d 1321 (Fed. Cir. 1998); Electro Medical Systems S.A. v. Cooper Life Sciences, Inc., 34 F.3d 1048, 32 USPQ2d 1017 (Fed. Cir. 1994).
[2] In re Rijckaert, 9 F.3d 1531, 28 USPQ2d 1955 (Fed. Cir. 1993); Lindermann Maschinenfabrik GMBH v. American Hoist & Derrick Co., 730 F.2d 1452, 221 USPQ 481 (Fed. Cir. 1984).
[3] Lindermann Maschinenfabrik GMBH v. American Hoist & Derrick Co., supra.

22. In contrast, as illustrated in Fig. 1 of Applicant's disclosure, a void 41 separates a plug 31 from a second interconnection 12. Therefore, Lee fails to identically disclose the claimed invention, as recited in claim 1, within the meaning of 35 U.S.C. § 102.

With regard to claims 2 and 4, the Examiner stated that Lee discloses "a second interconnection 22 having a barrier metal layer and an aluminum interconnection." In response, Applicant submits that the Examiner's failed to clearly designate the teachings in the reference being relied upon by the Examiner. In this regard, the Examiner's rejection fails to comport to the provisions of 37 C.F.R. § 1.104(c).[4] A review of Lee fails to yield where the conductive layer 22 includes a barrier metal layer and an aluminum interconnection. Lee only describes that the conductive layer can include "aluminum or copper" (column 3, lines 28-34). Thus, Lee further fails to identically disclose the limitations recited in claims 2 and 4.

The above argued differences between the semiconductor device defined in independent claim 1 and the device of Lee undermine the factual determination that Lee identically describes the claimed invention within the meaning of 35 U.S.C. § 102.[5] Applicant, therefore, respectfully submits that the imposed rejection of claims 1-5 and 8-12 under 35 U.S.C. § 102 for lack of novelty as evidenced by Lee is not factually viable and, hence, solicit withdrawal thereof.

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[4] 37 C.F.R. § 1.104(c) provides:

> In rejecting claims for want of novelty or for obviousness, the examiner must cite the best references at his or her command. When a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable. The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified.

[5] Minnesota Mining & Manufacturing Co. v. Johnson & Johnson Orthopaedics Inc., 976 F.2d 1559, 24 USPQ2d 1321 (Fed. Cir. 1992); Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 230 USPQ 81 (Fed. Cir. 1986).

Claims 6-7 and 13-14 are rejected under 35 U.S.C. § 102 for lack of novelty as evidenced by Lee

In the fourth enumerated paragraph of the Office Action, the Examiner asserted that Lee discloses a semiconductor device corresponding to that claimed. This rejection is respectfully traversed.

Independent claim 6, as amended, recites that a predetermined void in a second dielectric film is located at a position directly over and above a plug. This feature, however, is not disclosed by Lee. The void 26b of Lee can be considered positioned above (i.e., higher than) the conductive plug 20 (see Fig. 1F); however, the void 26b is not located directly over the conductive plug 20. Instead, the void 26b is located to one side of the conductive plug 20. Therefore, Lee fails to identically disclose the claimed invention, as recited in independent claim 6, within the meaning of 35 U.S.C. § 102.

The above argued differences between the semiconductor device defined in independent claim 6 and the device of Lee undermine the factual determination that Lee identically describes the claimed invention within the meaning of 35 U.S.C. § 102. Applicant, therefore, respectfully submits that the imposed rejection of claims 6-7 and 13-14 under 35 U.S.C. § 102 for lack of novelty as evidenced by Lee is not factually viable and, hence, solicit withdrawal thereof.

Claims 15-18 are rejected under 35 U.S.C. § 103 for obviousness predicated upon Anma et al., U.S. Patent No. 6,319,812 (hereinafter Anma) in view of Nakagawa et al., U.S. Pub. No. 2002/0050651 (hereinafter Nakagawa)

In the sixth enumerated paragraph of the Office Action, the Examiner concluded that one having ordinary skill in the art would have been motivated to modify the semiconductor device of

Anma in view of Nakagawa to arrive at the claimed invention. This rejection is respectfully traversed.

In the statement of the rejection, the Examiner argued that one having ordinary skill in the art would have been motivated to modify Anma in view of Nakagawa in order to reduce parasitic capacitance. Applicant respectfully disagrees. Nakagawa describes the use of air gaps with multi-layer interconnects and high-aspect ratios. However, the interconnects 20 of Anma are neither multi-layer nor do they have high-aspect ratios. As such, the motivation to use air gaps with the multi-layer, high-aspect ratio interconnects of Nakagawa are inapplicable to the interconnects of Anma. Furthermore, the void of the claimed invention is located to form an anti-fuse structure and not to reduce parasitic capacitance.

Claim 16 recites that a second interconnection becomes narrower in a vicinity of a pad. This feature can be illustrated, for example, in Fig. 32 of Applicant's disclosure, which discloses that a second interconnection 15b becomes narrower in a vicinity of a plug 33.

On page 5 of the Office Action, the Examiner stated:

> Regarding claim 16, Lee discloses a second interconnection formed so as to become narrow in the vicinity of said plug.

The Examiner, however, has failed to clearly designate the particular teaching in Lee being relied upon by the Examiner for teaching this particular limitation. In this regard, the Examiner's rejection fails to comport to the provisions of 37 C.F.R. § 1.104(c). Furthermore, a review of Lee also fails to yield this particular limitation being attributed to Lee by the Examiner.

Lee has also been inappropriately applied by the Examiner as Lee has not been cited in the rejection under 35 U.S.C. § 103. However, even if the Examiner properly cited Lee, the Examiner has failed to establish a motivation to modify Anma and Nakagawa in view of the teachings of Lee. Furthermore, even if Anma were modified in view of Nakagawa and Lee, the claimed invention would not result because none of the references, alone or in combination, teach or suggest a second interconnection becoming narrower at a vicinity of a plug. Applicant, therefore, respectfully submits that the imposed rejection of claims 15-18 under 35 U.S.C. § 103 for obviousness predicated upon Anma in view of Nakagawa and Lee is not viable and, hence, solicits withdrawal thereof.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "Version with markings to show changes made."

Applicant has made every effort to present claims which distinguish over the prior art, and it is believed that all claims are in condition for allowance. However, Applicant invites the Examiner to call the undersigned if it is believed that a telephonic interview would expedite the prosecution of the application to an allowance. Accordingly, and in view of the foregoing remarks, Applicant hereby respectfully requests reconsideration and prompt allowance of the pending claims.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper,

including extension of time fees, to Deposit Account 500417, and please credit any excess fees to such deposit account.

Respectfully submitted,

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Version with markings to show changes made

IN THE CLAIMS:

1. (Twice Amended) A semiconductor device comprising:

a substrate;

a first interconnection formed on said substrate;

a first dielectric film covering said first interconnection;

an opening section extending from a surface of the first dielectric film to said first interconnection, said opening section being formed in said first dielectric film;

a plug formed in said opening section and electrically connected to said first interconnection;

a second interconnection formed over said plug;

a predetermined void between said plug and said second interconnection; and

a second dielectric film covering said second interconnection, wherein said predetermined void separates said plug from said second interconnection.

6. (Twice Amended) A semiconductor device comprising:

a substrate;

a first interconnection formed on said substrate;

a first dielectric film covering said first interconnection;

an opening section extending from a surface of said first dielectric film to said first interconnection, said opening section being formed in said first dielectric film;

a plug formed in said opening section and electrically connected to said first interconnection;

a second interconnection formed on said first dielectric film in the vicinity of said plug ;

a second dielectric film covering said second interconnection; and

a predetermined void in said second dielectric film and located at a position adjacent to said second interconnection and at a position directly over and above said plug.